# LESSON PLAN

**Subject Code & Name: DSPA**

**Branch: VLSI Class / Semester: IM.Tech-SEM II Academic Year:2013-14**
**Faculty: J.Swathi**

| Period | Date (Tentative) | Topic | Unit No. | Teaching Methodology | Remarks | Corrective action upon review |
|---|---|---|---|---|---|---|
| | | **DESIGN OF DIGITAL SYSTEMS** | **I** | | | |
| 1 | 14.02.2014 | Introduction To digital signal processing | | BB | | |
| 2 | 19.02.2014 | digital signal processing system | | BB | | |
| 3 | 20.02.2014 | Sampling process, discrete time sequences | | BB | | |
| 4 | 20.02.2014 | discrete fourier transforms | | BB | | |
| 5 | 21.02.2014 | fast fourier transforms, LTI Systems | | BB | | |
| 6 | 26.02.2014 | Digital filters ,decimation and interpolation | | BB | | |
| | | **COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS** | **II** | | | |
| 7 | 27.02.2014 | Introduction | | BB | | |
| 8 | 27.02.2014 | Number formats for signal and coefficients | | BB | | |
| 9 | 28.02.2014 | Dynamic range and precision, examples | | BB | | |
| 10 | 05.03.2014 | Sources of errors in DSP Implementations A/D conversions | | BB | | |
| 11 | 06.03.2014 | DSP computational errors | | BB | | |
| 12 | 06.03.2014 | D/A conversion Errors,compensating filters | | BB | | |
| | | **ARCHITECTURES FOR PROG DSP DEVICES** | **III** | | | |
| 13 | 07.03.2014 | Basic architectural features | | BB | | |
| 14 | 12.03.2014 | DSP Computational building blocks,multiplier,MAC | | BB | | |
| 15 | 13.03.2014 | ALU, Shifter, Barrel shifter | | BB | | |
| 16 | 13.03.2014 | Bus architecture & memory Address Generation unit | | BB | | |
| 17 | 14.03.2014 | Data addressing capabilities | | BB | | |
| 18 | 19.03.2014 | Programmability, prog execution | | BB | | |
| 19 | 20.03.2014 | H/W looping , interrupts | | BB | | |
| 20 | 20.03.2014 | Pipeling and performance | | BB | | |
| 21 | 21.03.2014 | Branching effects and interrupt effects | | | | |
| 22 | 26.03.2014 | Pipeline programming models | | | | |
| | | **PROGRAMMABLE DIGITAL SIGNAL PROCESSORS** | **IV** | | | |

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|---|---|---|---|---|---|---|
| 23 | 27.03.2014 | Commercial DSP's | | BB | | |
| 24 | 27.03.2014 | Architecture of TMS320C54XX | | BB | | |
| 25 | 02.04.2014 | Data addressing modes of TMS320C54XX | | BB | | |
| 26 | 03.04.2014 | Memory space of TMS320C54XX processor | | BB | | |
| 27 | 03.04.2014 | TMS320C54XX instructions and programming examples | | BB | | |
| 28 | 04.04.2014 | On chip pheripherals ,timers,counter interrupts | | BB | | |
| 29 | 09.04.2014 | Pipeline operation of TMS320C54XX | | BB | | |
| 30 | 10.04.2014 | The Q-notation implementation of FFT alogorithms | **V** | BB | | |
| 31 | 10.04.2014 | FIR filters, IIR filters | | BB | | |
| 32 | 11.04.2014 | Interpolation and decimation filters | | BB | | |
| 33 | 16.04.2014 | PID controller, Adaptive filters | | BB | | |
| 34 | 17.04.2014 | 2-D signal processing fft | | BB | | |
| 35 | 17.04.2014 | Butterfly computation,overflow and scaling | | | | |
| 36 | 18.04.2014 | Bit reversed index generation ,computation of the signal processing | | BB | | |
| 37 | 23.04.2014 | An 8-point FFT implementation of the TMS320C54XX | | BB | | |
| 38 | 24.04.2014 | Interfacing memory and I/O pheripherals | **VI** | | | |
| 39 | 24.04.2014 | Memory space org, external bus | | BB | | |
| 40 | 25.04.2014 | Memory interface,parallel i/o interface | | BB | | |
| 41 | 22.05.2014 | Programmed i/o interrupts | | BB | | |
| 42 | 23.05.2014 | DMA | | BB | | |
| 43 | 24.05.2014 | MCBSP | | BB | | |
| 44 | 28.05.2014 | CODEC | | BB | | |
| 45 | 29.05.2014 | CODEC-DSP interface, examples | | BB | | |

**CR: CLASS ROOM** **PPT: POWER POINT PRESENTATION** **LCD**

**TEXT BOOKS:**

1.Digital Signal Processing Implementations: Using DSP Microprocessors--With Examples from TMS320C54xx. by Avtar Singh, S. Srinivasan

2. Digital Signal Processing Implementations: Using DSP Microprocessors--With Examples from TMS320C54xx. S. Srinivasan

**FACULTY** **HEAD OF THE DEPARTMENT**