

LESSION PLAN

| Period | Date (Tentative) | Topic | Unit No. | Teaching Methodology | Remarks | Corrective Action Upon Review |
|--------|---------------------|--|-------------|-------------------------|---------|----------------------------------|
| | | <u>UNIT - I</u> | | | | |
| | | <u>BASIC CONCEPTS</u> | I | | | |
| 1 | 13.02.14 | Reliability concepts | | CR | | |
| 2 | 14.02.14 | Failure & Faults | | CR | | |
| 3 | 15.02.14 | Reliability & Failure Rate | | CR | | |
| 4 | 20.02.14 | Relation b/w reliability & mean time b/w failure | | CR | | |
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| 5 | 24.02.14 | Maintainability b/w and Availability | | CR | | |
| 6 | 22.02.14 | Reliability of series, parallel | | CR | | |
| 7 | 28.02.14 | Reliability of parallel series combination circuit | | CR | | |
| | | <u>UNIT - II</u> | | | | |
| | | <u>FAULT TOLERANT DESIGN</u> | II | | | |
| 8 | 01.03.14 | Static, Dynamic system | | CR | | |
| 9 | 06.03.14 | Hybrid, triple modular Redundant system | | CR | | |
| 10 | 07.03.14 | Self purging Redundancy | | CR | | |
| 11 | 08.03.14 | Self out Redundancy (SMR) | | CR | | |
| 12 | 13.03.14 | SMR configuration | | CR | | |
| 13 | 14.03.14 | Use of Error correcting code | | CR | | |
| 14 | 15.03.14 | Time Redundancy | | CR | | |
| 15 | 20.03.14 | Soft with Redundancy | | CR | | |

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| | | <u>UNIT - III</u> | | | | |
| | | <u>SELF CHECKING CIRCUITS</u> | <u>III</u> | | | |
| 16 | 21.03.14 | Basic concepts of self checking circuits | | CR | | |
| 17 | 22.03.14 | Design of Totals self checking checker | | CR | | |
| 18 | 23.03.14 | checker using m out of n codes | | CR | | |
| 19 | 03.04.14 | Berger code | | CR | | |
| 20 | 04.04.14 | Low cost encoder code | | CR | | |
| | | <u>UNIT - IV</u> | | | | |
| | | <u>FAIL SAFE DESIGN</u> | <u>IV</u> | | | |
| 21 | 05.04.14 | Strongly Fault secure circuits | | CR | | |
| 22 | 12.04.14 | Fail safe design of sequential circuits using partition theorem | | CR | | |
| 23 | 19.04.14 | Berger code | | CR | | |
| 24 | 24.04.14 | Totals self checking PLA design | | CR | | |
| | | <u>UNIT - V</u> | | | | |
| | | <u>DESIGN FOR TESTABILITY FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS</u> | <u>V</u> | | | |
| 25 | 25.04.14 | Basic concepts of Testability | | | | |
| 26 | 26.04.14 | controllability & observability | | | | |
| 27 | 02.05.14 | The Reed Miller's Expanding Technique | | | | |

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| 28 | 03.05.14 | OR-AND-NOR design | V | CR | | |
| 29 | 22.05.14 | Use of control and syndrome testable design | | CR | | |
| 30 | 23.05.14 | Control bits and observability by means of scan and register storage cell for design | | CR | | |
| 31 | 24.05.14 | Linear scan design | | CR | | |
| 32 | 29.05.14 | Level sensitive scan design (LSSD) | | CR | | |
| | | UNIT - VI | VI | | | |
| 33 | 30.05.14 | Theory and operation of LFSR | | CR | | |
| 34 | 04.06.14 | LFSR as signature Analyzer | | CR | | |
| 35 | 05.06.14 | Multiple input signature Register | | CR | | |
| | | <u>BUILT IN SELF TEST</u> | | | | |
| 36 | 07.06.14 | BIST concepts | | CR | | |
| 37 | 12.06.14 | Test pattern generation for BIST Exhaustive testing | | CR | | |
| 38 | 13.06.14 | Pseudo random testing | | CR | | |
| 39 | 14.06.14 | Pseudo exhaustive testing | | CR | | |
| 40 | 19.06.14 | Comp weight patterns | | CR | | |
| 41 | 20.06.14 | Generic off-line BIST Architecture | | CR | | |
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