LESSION PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1		ROM Features, Architectures	1			
2		ROM Programming	1			
3		PLA Features, Architectures	1			
4		PLA Programming	1			
5		PAL features, architectures	1			
6		PAL Programming	1			
7		CPLD features, architecture	1			
8		CPLD Programming	1			
9		FPGIA features, architecture	1			
10		FPGIA Programming	1			
11		Applications & implementation of MSI CKTs using PLD	1			
12		CPLDs – Complex Programmable logic devices	2			
13		Altera series – Max 5000/ 7000 series	2			
14		Altera FLEX logic – 10000 series CPLD	2			
15		AMD's – CPLD (mach 1 to 5)	2			
16		Cypress FLASH 370 device technology	2			
17		Lattice PLSI's architectures 3000 series	2			
18		Speed performance & in System Programmability	2			
19		FPGAs: Field Programmable Gate arrays	3			
20		FPGA: Logic blocks	3			

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
21		FPGA – routing architecture	3			
22		FPGA – design flow	3			
23		Technology mapping for FPGAs	3			
24		Case studies xilinx XC4000	3			
25		ALTERA'S FLEX 8000/ 10000	3			
26		FPGAS: AT&T ORCA'S	3			
27		TOP Down Design, State transition table	4			
28		State assignments for FPGAS, realization of state machine charts using PAL	4			
29		Alternative realization for state machine charts using microprogramming	4			
30		linked state machine, encoded state machine	4			
31		Architectures Centered around non registered PLDS	4			
32		Design of State machines Centered around shift registers	4			
33		one hot state machine, Petrinets for state machines	4			
34		Basic Concepts and Properties	4			
35		Finite state machine – Case Study	4			
36		One hot design method	5			
37		Use of ASMs in one-hot design method	5			
38		Applications of Onehot design method	5			
39		Extended Petrinets for Parallel Controllers	5			
40		meta Stability & Synchronization	5			

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
41		Complex design using shift registers	5			
42		System level Design : Controller	6			
43		Data Path designing	6			
44		Functional Partition	6			
45		Digital front end digital design tools for FPGAS & ASICS	6			
46		System level design using mentor graphics EDA tool	6			
47		Design flow using CPLD & FPGAs	6			
48		Design Considerations using CPLDS	6			
49		Design Considerations using FPGAS of 11th adder	6			
50		Parallel adder	6			
51		sequential circuits	6			
[illegible]		Counters	6			
[illegible]		multiplexers	6			
[illegible]		Parallel Controllers	6			